WHAT IS CLAIMED IS:

1. An active matrix display device comprising:

an active matrix circuit and a driver circuit formed over a substrate;

said driver circuit including at least a first thin film transistor and a second thin film transistor;

said first thin film transistor comprising:

a first semiconductor layer having first source and drain regions, a pair of lightly-doped regions and a first channel forming region therebetween;

a first gate electrode adjacent to said first channel forming region with a first gate insulating layer interposed therebetween, and

said second thin film transistor comprising:

a second semiconductor layer having second source and drain regions and a second channel forming region therebetween;

a second gate electrode adjacent to said second channel forming region with a second gate insulating layer interposed therebetween,

wherein said second channel forming region directly contacts with said second source and drain regions, and

wherein a pair portions containing n-type and p-type impurities are formed adjacent to said second source region and said second drain region

2. An active matrix display device comprising:

an active matrix circuit and a driver circuit formed over a substrate;

said driver circuit including at least a first thin film transistor and a second thin film transistor;

said first thin film transistor comprising:

a first semiconductor layer having first source and drain regions, a pair of lightly-doped regions and a first channel forming region therebetween;

a first gate electrode adjacent to said first channel forming region with a first gate insulating layer interposed therebetween, and

said second thin film transistor comprising:

a second semiconductor layer having second source and drain regions and a second channel forming region therebetween;

a second gate electrode adjacent to said second channel forming region with a second gate insulating layer interposed therebetween,

wherein said second source and drain regions contain p-type impurity and directly connect with said second channel forming region, and

wherein a pair of portions containing n-type and p-type impurities are formed adjacent to said second source region and said second drain region.

3. An active matrix display device comprising:

an active matrix circuit and a driver circuit formed over a substrate;

said driver circuit including at least one thin film transistor, said thin film transistor comprising:

a semiconductor layer having a source and drain regions and a channel forming region therebetween; and

a gate electrode adjacent to said channel forming region with a gate insulating layer interposed therebetween,

wherein said channel forming region directly contacts with said second source and drain regions, and

wherein a pair of portions containing n-type and p-type impurities are formed adjacent to said source and drain region.

4. An active matrix display device comprising:

an active matrix circuit and a driver circuit formed over a substrate;

said driver circuit including at least one thin film transistor, said thin film transistor comprising:

a semiconductor layer having a source and drain regions and a channel forming region therebetween; and

a gate electrode adjacent to said channel forming region with a gate insulating layer interposed therebetween,

wherein said source and drain regions contain p-type impurity and directly connect with said channel forming region, and

wherein a pair of portions containing n-type and p-type impurities are formed adjacent to said source and drain region.

5. An active matrix display device according to any one of claims 1 to 4, wherein said first source and drain regions contain an n-type impurity.

6. An active matrix display device according to any one of claims 1 to 4, wherein said first and second channel forming regions contain an impurity imparting one conductivity.

7. An active matrix display device according to any one of claims 1 to 4, wherein said first and second semiconductor layers contain hydrogen and halogen.

8. A semiconductor device having at least one thin film transistor formed over a substrate, said thin film transistor comprising:

a semiconductor layer having a source and drain regions and a channel forming region therebetween;

a gate electrode adjacent to said channel forming region with a gate insulating layer interposed therebetween,

wherein said channel forming region directly contacts with said second source and drain regions, and

wherein a pair of portions containing n-type and p-type impurities are formed adjacent to said source and drain region.

9. A semiconductor device having at least one thin film transistor formed over a substrate, said thin film transistor comprising:

a semiconductor layer having a source and drain regions and a channel forming region therebetween;

a gate electrode adjacent to said channel forming region with a gate insulating layer interposed therebetween,

wherein said source and drain regions contain p-type impurity and directly contact with said channel forming region, and

wherein a pair of portions containing n-type and p-type impurities are formed adjacent to said source and drain region.

10. A semiconductor device according to either one of claim 8 or 9, wherein said channel forming region contains an impurity imparting one conductivity.

11. A semiconductor device according to either one of claim 8 or 9, wherein said semiconductor layer contains hydrogen and halogen.